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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,647	06/28/2001	Joo Soo Lim	8733.442.00	2011

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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2673	4

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,647	LIM, JOO SOO	
	Examiner	Art Unit	
	Prabodh M Dharia	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 11 is objected to because of the following informalities: Claim 11 does not end with "." period. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8,10,12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita (6,275,061 B1) in view of Firester et al. (6,611,241 B1).

Regarding Claim 1, Tomita teaches a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and a plurality of liquid crystal pixel cells (Col. 8, Lines 12,13) arranged where the gate lines cross the data lines (Col. 4, Lines 45-64), the method comprising: applying data

voltages to the data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53-55); applying a mode setting signal to a gate driver connected with the gate lines; sequentially scanning the gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel (Col. 8, Lines 48-65); and identifying any defective pixel cells among the plurality of liquid crystal pixel cells from the test pattern (Col. 7, Lines 50-56). teaches a liquid crystal display device (Col. 3, Lines 45,46), comprising: a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of scanning lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and liquid crystal pixel cells arranged in a matrix (Col. 3, Lines 54,55, Col. 8, Lines 12,13); a data driver circuit for supplying data to the data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53-55); a scanning driver circuit for supplying scanning signals to the scanning lines (Col. 17, Lines 40-53, Col. 19, lines 39-50, Col. 15, Lines 51-58, Col. 13, Lines 31,32); and control means for controlling the data driver circuit and the scanning driver circuit (Col. 3, Lines 55-57, Col. 4, Lines 57-59), wherein said control means controls the scanning driver circuit (Col. 8, Lines 26-65).

However, Tomita fails to teach sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device.

However, Firester et al teaches sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device (Col. 17, Lines 40-53, Col. 19, lines 39-50, Col. 15, Lines 51-58, Col. 13, Lines 31,32).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Firester et al. teaching in teaching of Tomita to be able to forming or testing in

two contiguous pixeleted sub-images having a region of overlap at their common edges and determining the value (defects) of particular pixels in the region for correction purposes.

Regarding Claim 2, Tomita teaches a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and a plurality of liquid crystal pixel cells (Col. 8, Lines 12,13) arranged where the gate lines cross the data lines (Col. 4, Lines 45-64).

Regarding Claim 3, Tomita teaches switching device consists of a thin film transistor (Col. 4, Lines 47,48) including a gate electrode connected to a corresponding one of the scanning lines to receive the scanning signal (Col. 3, Lines 55-57, Col. 4, Lines 57-59); a source electrode connected to a corresponding one of the data lines to receive said data (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54); and a drain electrode opposed to the source electrode with a desired channel there between and connected to a pixel electrode for driving the liquid crystal pixel cell (Col. 6, Lines 24-41, P-channel and N channel Col. 4, Lines 53-67).

Regarding Claim 4, Tomita teaches control means generates a gate start pulse for indicating a start position of the scanning signal, a mode setting signal for assigning an application direction of the scanning signal to any one of a forward direction and a reverse direction, and an output enable signal for controlling an output of the scanning driver circuit (Col. 8, Lines 35-41, Col. 8, Lines 26-65, Col. 9, Line 62 to Col. 10, Line 3).

Regarding Claim 5, Tomita teaches control means applies a dot clock for indicating an application time of said data to the data driver circuit (Col. 8, Lines 35-41).

Regarding Claim 6, Tomita teaches scanning driver circuit consists of a bilateral shift resistor in which its shift direction is controlled in response to a mode setting signal (Col. 8, Lines 26-65, Col. 9, Line 62 to Col. 10, Line 3)

Regarding Claim 7, Tomita teaches control means controls the scanning driver circuit such that the liquid crystal display panel is scanned in a forward-sequential manner upon normal operation of the liquid crystal display panel (Col. 8, Lines 48-65).

Regarding Claim 8, Tomita teaches a method of testing a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and scanning the scanning lines in a sequence proceeding from low-order lines to high-order lines to display a test picture (Col. 8, Lines 48-65); and identifying any defective pixel cells among the plurality of liquid crystal pixel cells from the test pattern (Col. 7, Lines 50-56).

However, Tomita fails to teach sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device.

However, Firester et al teaches sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device (Col. 17, Lines 40-53, Col. 19, lines 39-50, Col. 15, Lines 51-58, Col. 13, Lines 31,32).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Firester et al. teaching in teaching of Tomita to be able to forming or testing in two contiguous pixeleted sub-images having a region of overlap at their common edges and determining the value (defects) of particular pixels in the region for correction purposes.

Regarding Claim 10, applying a mode setting signal to a gate driver connected with the gate lines; sequentially scanning the gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel (Col. 8, Lines 48-65). Firester et al teaches reverse mode is set by a mode setting signal that is applied to a scanning driver circuit generating a scanning signal, to thereby indicate an application direction of the scanning signal (Col. 17, Lines 40-53, Col. 19, lines 39-50, Col. 15, Lines 51-58, Col. 13, Lines 31,32).

Regarding Claim 12, Tomita teaches a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and a plurality of liquid crystal pixel cells (Col. 8, Lines 12,13) arranged where the gate lines cross the data lines (Col. 4, Lines 45-64), the method comprising: applying data voltages to the data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53-55); applying a mode setting signal to a gate driver connected with the gate lines; sequentially scanning the

gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel (Col. 8, Lines 48-65).

However, Tomita fails to teach sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device.

However, Firester et al teaches sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device (Col. 17, Lines 40-53, Col. 19, lines 39-50, Col. 15, Lines 51-58, Col. 13, Lines 31,32).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Firester et al. teaching in teaching of Tomita to be able to forming or testing in two contiguous pixeleted sub-images having a region of overlap at their common edges and determining the value (defects) of particular pixels in the region for correction purposes.

Regarding Claim 13, Tomita teaches the gate driver circuit comprises a shift register having a control terminal for controlling a sequential order of supplying the gate signal to the gate lines (Col.8, Lines 48-65)

Regarding Claim 14, Tomita teaches a controller supplying a mode-setting signal to the control terminal (Col. 8, Lines 26-51).

5. Claims 9,11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita (6,275,061 B1) in view of Firester et al. (6,611,241 B1) as applied to claims 1-8,10,12-14 above, and further in view of Asada et al. (5,883,609).

Regarding Claim 9, Tomita teaches scanning the scanning lines includes driving a drive circuit for driving said low-order lines and thereafter driving a drive circuit for driving said high-order lines (Col. 8, Lines 48-65).

However, Tomita modified by Firester et al. fails to teach specifically scanning the scanning lines in a sequence proceeding from low-order lines to high-order lines comprises shifting a shift register in a reverse direction from.

However, Asada et al. teaches scanning the scanning lines in a sequence proceeding from low-order lines to high-order lines comprises shifting a shift register in a reverse direction from (Col.6, Lines 54-56, Col.7, Lines 40-54, Col. 8, Lines 4-36).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Asada et al. teaching in teaching of Firester et al. to be able to reduce increased noises and/or differences of timing between control signals tend to deteriorate a signal to noise ratio of an output signal; and provide a practical multi-purpose LCD of which peripheral drive circuit is operative with a relatively small number of control signal terminals (mode setting signal), permitting an improved SN ratio, an effective size reduction and an improved cost effects.

Regarding Claim 11, Asada et al. teaches scanning the scanning lines in a sequence proceeding from low-order lines to high-order lines comprises shifting a shift register in a reverse direction from (Col.6, Lines 54-56, Col.7, Lines 40-54, Col. 8, Lines 4-36).

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita (6,275,061 B1) in view of Henley et al. (US RE37,847 E).

Regarding Claim 15, Tomita teaches a method of testing a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and a plurality of liquid crystal pixel cells (Col. 8, Lines 12,13) arranged where the gate lines cross the data lines (Col. 4, Lines 45-64), the method comprising: applying data voltages to the data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53-55); applying a mode setting signal to a gate driver connected with the gate lines; sequentially scanning the gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel (Col. 8, Lines 48-65); and identifying any defective pixel cells among the plurality of liquid crystal pixel cells from the test pattern (Col. 7, Lines 50-56).

However, Tomita fails to teach specifically testing of the pixel defectiveness using test pattern.

However. Henley et al. teaches testing of the pixel defectiveness using test pattern (Col. 2, Lines 34-36).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Henley et al. teaching in teaching of Tomita to be able to test a LCD panel arrays for open circuit and pixel defects by applying test signals to panel shorting bars.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is informed that all of the other additional cited references either anticipate or render the claims obvious. In order to not to be repetitive and exhaustive, the examiner did draft additional rejection based on those references.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Henley (5,432,461) Method of testing active matrix Liquid crystal display substrates.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU2673

July 29,2004

VIJAY SHANKAR
PRIMARY EXAMINER